Single Event Effects Test Results for the Actel ProAsic Plus and Altera Stratix-II Field Programmable Gate Arrays

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Abstract—This work describes radiation testing of Actel's ProASIC Plus and Altera's Stratix-II FPGAs. The Actel Device Under Test (DUT) was a ProASIC Plus APA300-PQ208 nonvolatile, field reprogrammable device which is based on a 0.22um flash-based LVCMOS technology. Limited investigation has taken place into flash based FPGA technologies, therefore this test served as a preliminary reference point for various SEE behaviors. The Altera DUT was a Stratix-II EP2S60F1020C4. Single Event Upset (SEU) and Single Event Latchup (SEL) were the focus of these studies. For the Actel, a latchup test was done at an effective LET of 75.0 MeV-cm^2/mg at room temperature, and no latchup was detected when irradiated to a total fluence of 1x10^7 particles/cm^2. The Altera part was shown to latchup at room temperature.

Index Terms—Field Programmable Gate Arrays, Heavy Ions, Single Event Latchup, Single Event Upsets.

I. INTRODUCTION

THE prospect of using reprogrammable devices in space is one that appeals to many designers due to lower development cost (compared to one time programmable FPGAs) and the ability to reconfigure or adapt a design at all stages of a mission. Re-configurability comes at a cost of upset mitigation due to the intrinsically "soft" nature of many of these devices. The three primary vendors of FPGAs are Altera, Xilinx and Actel. Much work has been done to investigate Single Event Effects (SEE) and SEE mitigation techniques of the Xilinx SRAM-based FPGAs (Virtex-II family) [1], [7]. Altera's SRAM-based FPGAs (Stratix family) have been tested and thus far proven to be extremely sensitive to latchup [2]. These experiments evaluate advanced Actel

FPGA's for applications in space as well as a next generation Altera Stratix part for latchup characteristics.

II. DEVICE CHARACTERISTICS

A) Actel ProAsic Plus

The Actel ProASIC family differs functionally from its counterparts in the fact that, rather than using SRAM configuration cells, it is a flash-based, non-volatile device, therefore not requiring external boot-up PROMs to support the device's configuration. A single flash switch consists of a pair of transistors that share a floating gate that stores the program bit. The first transistor writes and verifies the floating gate voltage, and the second is the switching transistor. Flash memory cells are used for routing and assigning and logic values. Also, one can clear the design by erasing the flash cells by removing the charge stored by the floating gate. This switch configuration leads to the conclusion that the flash-based FPGA may be less vulnerable to upsets than their SRAM counterparts due to a smaller physical switch size (two transistors as opposed to six) and a higher voltage potential on the floating gate [3, 4].
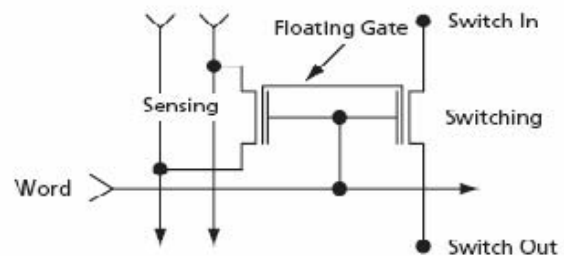

Fig. 1.   Schematic representation of the Flash Switch Architecture of the Pro Asic Plus device from [4]

The irradiated Actel DUT consisted of 300,000 system gates with 290 user I/O's, and 32 embedded block RAMs (each consisting of 72k-Bits). The DUT can be broken down into 8,192 tiles (registers) which can be configured as a flip-flop, latch, or a three input/one output logic device. The device operates with a 2.5V core voltage and supports either 2.5V or 3.3V I/O voltages.

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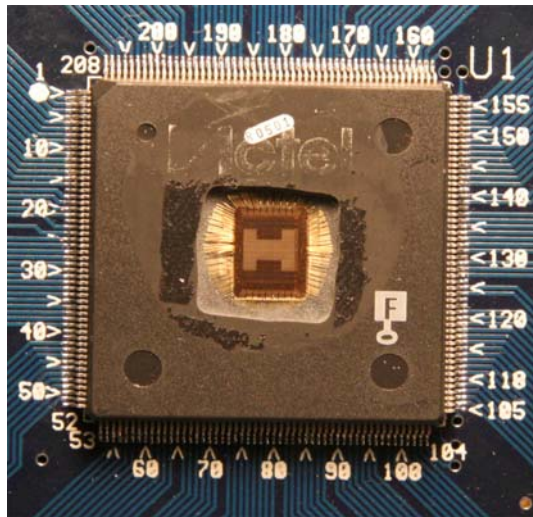
B)Altera Stratix-II

The Altera Stratix-II is a 1.2V core, 90-nm, SRAM based FPGA. The device structure is a two-dimensional row- and column-based architecture that provides signal interconnections between logic array blocks (LABs), memory structures, and DSP blocks. The LABs consist of eight adaptive logic modules (ALMs), which implements user logic. The use of I/O blocks provides the device with an interface from package pins to the internal signal lines. Re-configurability is established by programming the internal memory cells which determine the interconnects and logic functions of the FPGA.

The irradiated DUT consists of 48,352 logic elements (ALMs), 2,544,192 total ram bits, 36 DSP blocks, 144 embedded multipliers, 8 phase locked loops, and 718 user I/O's.

III. HARDWARE PREPARATION

A) Actel ProAsic Plus

Actel evaluation boards were used for development and testing. The FPGA design goal was to fill the device with four serial shift registers in order to shift in various patterns to observe upsets. To do this it was necessary to interface the DUT board with a Service Board that provides the DUT with the various desired patterns (ones, zeros, and checkerboard) as well as the shift register clock; the Service Board is designed to detect upsets. The use of this board limited the speed that we could clock the shift register and detect errors to a few hundred kHz. When the two boards were interfaced, terminating resistors were used on the signals for shift-in and shift-out as well as the clock to help reduce reflections. Three APA300s were de-lidded by the use of an acid etching machine and replaced the FPGAs on the development board.

(a)
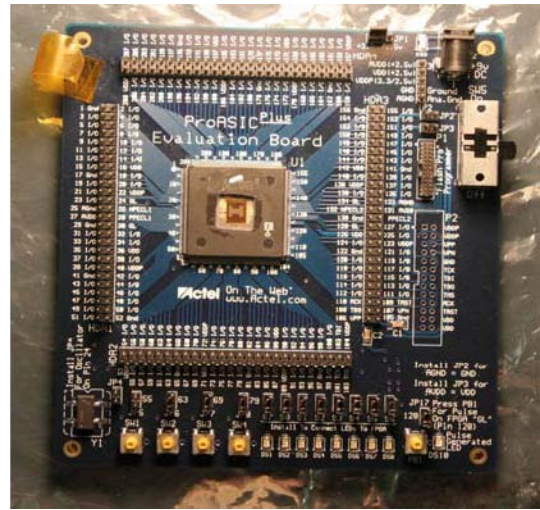
(b)

Fig. 2.   (a) The delidded DUT and with die exposed. (b) The evaluation board used for testing.

B)Altera Stratix-II

Altera DSP evaluation boards were used for development and testing. A similar FPGA design to that of the Actel test was used in order to verify functionality and if no latchup occurred, record upsets. In a similar manner, a Service board was used to provide shift register patterns, clock and reset, and to detect upsets. The Stratix-II parts were flip-chip, so three devices were de-lidded and the silicon thinned to approximately 50μm.

The devices were sent along with the development board to an assembly house to have the original parts removed and the thinned parts mounted. Hardware verification was performed upon return of the boards.
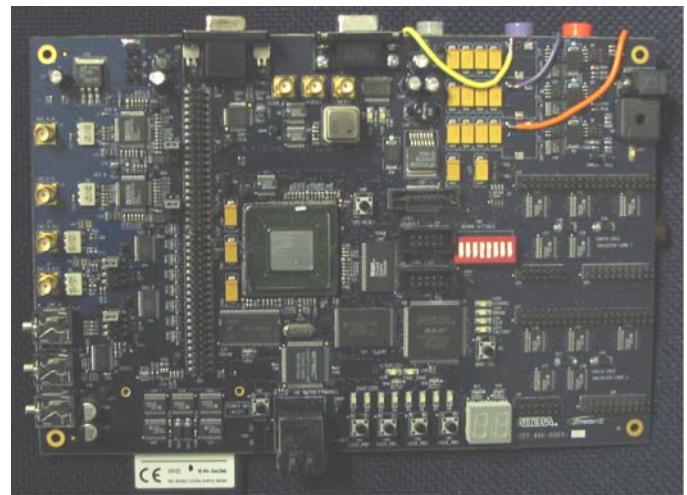
Fig. 3.   The evaluation board used for testing with the thinned DUT in the center.

IV. SOFTWARE DEVELOPMENT

The VHDL developed for each of these tests was straightforward. The Actel design consists of four 1023-bit shift registers with a built in synchronous reset. It is important

to note that the reset signal fanned out to every flip-flop in each shift register and when asserted sets the flip-flop output to a logic one. The clock was also fanned out to every flip-flop of every shift register in the design. Actel's IDE interpreted the code and developed a shift register that consisted of a series of alternating reset logic followed by flip-flops (as seen in figure three). As previously noted, the APA300 consists of 8192 register tiles, 8184 of which were used in the design.
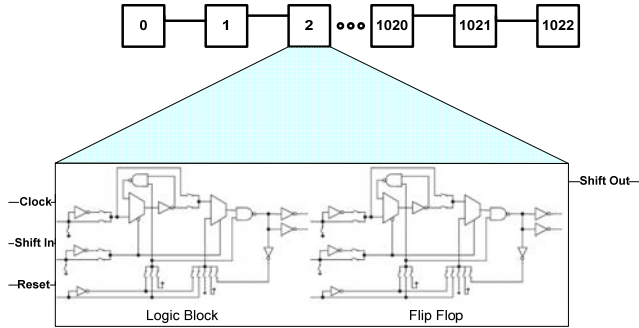

Fig. 4. Detection strategy for single events in the Actel test setup; one tile is used for the reset logic, and the second the register.

Similarly, the Altera design consisted of four 2048-bit shift registers with synchronous reset. The design used 4,096 ALMs, 16% of the total.

V.   TEST SETUP AND PROCEDURE

The test setup for both experiments is shown in figure four. A laptop was used in conjunction with a GPIB interface to control a four channel programmable power supply. The voltage regulators on the board were bypassed in order to monitor and control voltages and currents manually. A custom Visual Basic program was used to control voltages and currents as well as to monitor SEL. A current limit was set to detect SEL via the custom software. Nominal voltages were supplied to the DUT. A Function Generator was used to supply the Service Board with a square wave to serve as the design's clock in the case of the Actel test. The clock was generated form the Service Board in the case of the Altera test. The Service Board compared the shifted pattern out with the signal that was being shifted in, and sent error pulses out a 40-pin ribbon cable via receiver/driver cards to a custom-built counter board. The counter board separately counted the errors in the shift registers and sends them to the functional monitor laptop where the errors are recorded and displayed in a strip chart of the accumulating errors using a Visual Basic interface program.

The Visual Basic program, in conjunction with the counter board, also allows the experimenter to control what pattern is being sent into the shift register by way of the Service Board.

A routine was followed during the test after each beam run to verify functionality of the DUT. Power was cycled from one run to the next.
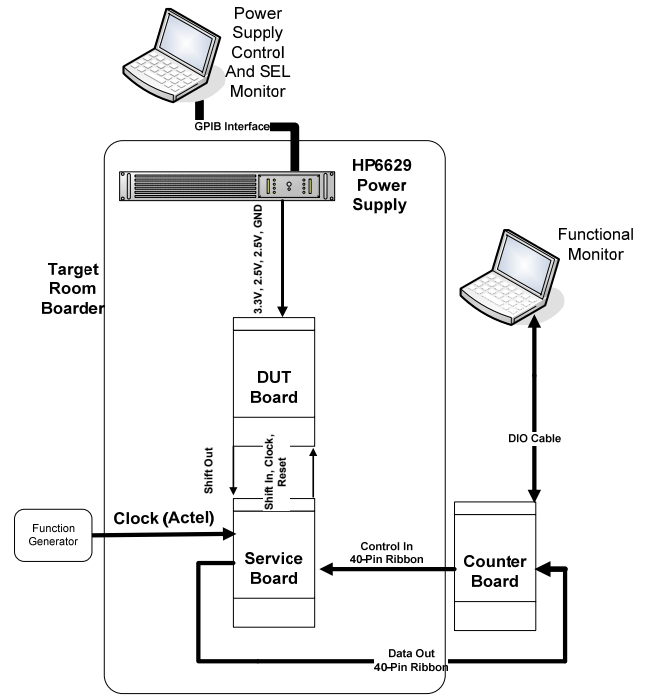

Fig. 5. Test Setup for both the Actel and Altera tests. For the Altera test, the function generator was not used as the clock was generated from the service board.

VI.   TEST RESULTS AND BEHAVIORAL OBSERVATIONS

A)   Actel ProAsic Plus

The goal of this test was to characterize the behavior of the ProAsic Plus in the beam. Possible SEE modes that the behavior and data were being analyzed for were: latchup, upsets, and "stuck bit" behavior. All test runs were done at room temperature in air with nominal voltages of 2.5V for the core, with V_{DDA} at 2.5V and V_{DDP} at 3.3V. Current limits for latchup detection were set to 200mA for the core and IO. No latchup events were observed with an LET of 75.0 MeV-cm^2/mg and a total fluence of $1x10^7$ particles/cm^2. Upsets were observed and recorded and is shown in figure five. Including the post irradiation pattern cycling, other post-beam analysis was done to verify that there was no catastrophic damage to the DUT, and no such damage could be found. In a test of this nature, SETs would be hard to single out, and if they did occur and were observable, they would appear within the upset data collected. It is unlikely that many SETs were recorded with this particular test setup because they must be clocked into the design and this design was running at a relatively slow rate.

An unusual behavior occurred during a test run when the checkerboard platform was selected to shift into the design. Upsets progressed gradually as was observed in the previous runs, then for a brief period the errors incremented in bursts of approximately 1023 upsets per read cycle (there are 32 read cycles per second). This behavior persisted for approximately six seconds, after which the errors accumulated at the expected, slower rate. This behavior began and ended in the first three shift register chains simultaneously, but the fourth

chain remained unaffected. This behavior can most likely be attributed to an upset induced timing error.

TABLE I
LIST OF THE IONS USED AT TAM

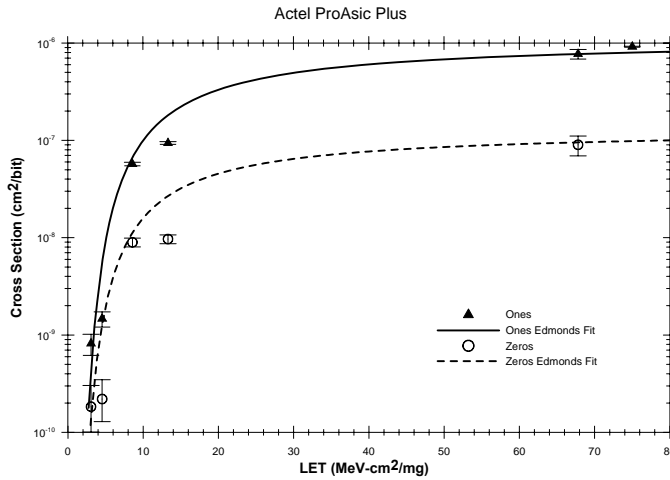| Ion	Energy (MeV)	Angle (Deg)	Degrader	LET (MeV-cm^2/mg)
Ne^{20}	300	0°	None	3.07
Ne^{20}	300	50°	None	4.55
Ar^{40}	599	0°	None	8.57
Ar^{40}	599	50°	None	13.3
Ag^{109}	1634	50°	None	67.8
Ag^{109}	1634	50°	1 at 36.1°	75

Fig. 6. Cross Section vs. LET for 0 → 1 upsets (zeros) and for 1 → 0 upsets (ones). Cross Sections fit with Edmonds fit [8], parameters Table II for fitting parameters.
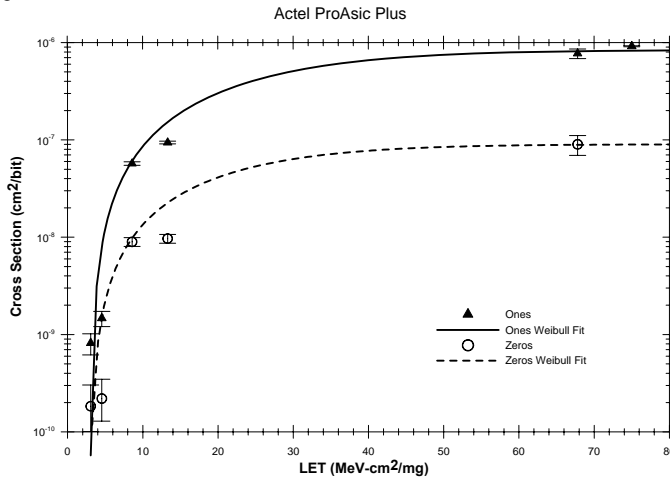

Fig. 7. Cross Section vs. LET for 0 → 1 upsets (zeros) and for 1 → 0 upsets (ones). Cross Sections fit with Weibull parameters, see Table II for fitting parameters.

TABLE II
LIST OF FITTING PARAMETERS
FOR ACTEL CROSS SECTIONS

Parameters	Edmonds		Weibull			
Data Pattern	L$_{1/e}$	σ$_{sat}$ MeV-cm^2/mg	Limit cm^2	Onset MeV-cm^2/mg	Width	Power
Ones	24	1.10E-06	8.34E-07	3.00	28.0	1.60
Zeros	21	1.30E-07	9.00E-08	2.99	23.6	1.50

B) Altera Stratix-II

The goal of this test was to verify or deny the existence of latchup behavior in the Stratix-II. A secondary goal was, if latchup was not a prevalent behavior, to collect upset data. All tests were done at the operating temperature in vacuum with nominal voltages of 1.2V on the core, with 2.5V and 3.3V set for the I/Os. The current limit for latchup detection was set to 750mA for the core.

TABLE III
LIST OF THE IONS USED AT BERKELEY

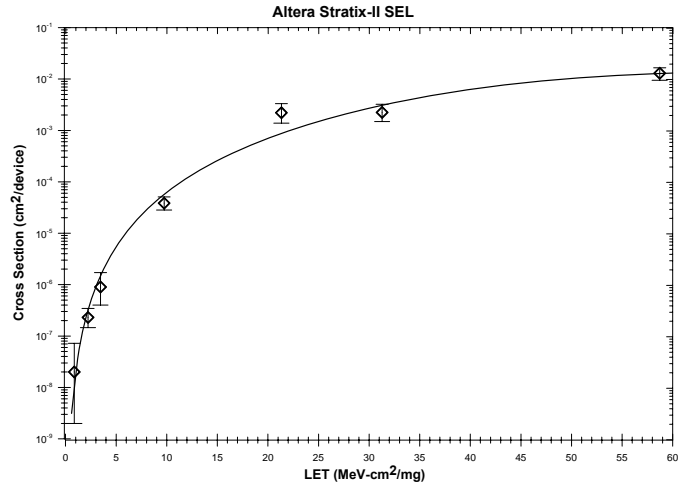| Ion	Energy (MeV)	Angle (Deg)	LET (MeV-cm^2/mg)
Xe^{38}	1403	0°	58.72
Kr^{24}	886	0°	31.28
Cu^{18}	659	0°	21.33
Ar^{11}	400	0°	9.74
Ne^6	216	0°	3.45
O^5	184	0°	2.22
B^3	108.2	0°	0.87

Fig. 8. Cross Section vs. LET for Altera Stratix-II SEL. Cross Section fit with Weibull parameters, see Table IV for fitting parameters.

TABLE IV
LIST OF FITTING PARAMETERS
FOR ALTERA CROSS SECTIONS

Weibull Parameters			
Limit (cm^2)	Onset (MeV-cm^2/mg)	Width	Power
1.80E-02	0.20	46.8	1.60

VII.   CONCLUSIONS AND FURTHER TESTING

The ProASIC Plus was not sensitive to latchp. The LET threshold is approximately 5 MeV-cm^2/mg, with a saturation cross section of about 10^{-7} cm^2/bit. Although this device does appear to be very SEU susceptible, work with SRAM-based Xilinx FPGAs has proven that mitigation techniques such as Triple Modular Redundancy (TMR) have made that technology viable for space flight. Another important test would include irradiating while the device is programming to detect SEGR or other related phenomena [3]. It would also be relevant to look into the upset-ability of the imbedded block RAMS, user I/O's, and PLL's, in addition to possible mitigation techniques of those components. Total Ionizing Dose (TID) would also be an appropriate test to pursue.

The Altera Stratix-II was sensitive to latchup events. The LET threshold for latchup was less than 1 MeV-cm^2/mg with a saturated cross section of about 10^{-2} cm^2/device.

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